Designing Switch Mode Power Supplies With the TL598

Application Report

TEXAS INSTRUMENTS

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Abstract

Designers of switching power supplies commonly specify MOSFET switches and therefore need control circuits with outputs capable of directly driving MOSFET switches. The TL598 control circuit was designed with this capability to avoid any need for additional output circuitry. After functionally describing the TL598, this report directs the designer through a complete dc-to-dc converter design using the TL598 as a pulse-width-modulation control circuit. Measurements of output and input regulation along with power efficiencies are included in table form to support the design example and point out the advantages of using the new TL598 device.

Introduction

Designers of switching power supplies commonly specify power MOSFET switches that operate at frequencies equal to or greater than 60 kHz, for the following reasons:

1. Reduction of power supply weight and size through improved magnetics
2. Reduction of complexity of power-switch drive circuitry

However, many of the standard control circuits, such as the TL494, are not configured for directly driving power MOSFET switches and extra output circuitry must be added. To eliminate this need for additional circuitry, the TL598 was designed. The TL598 contains two error amplifiers, an internal oscillator (externally adjustable), a dead-time control comparator, a pulse-steering flip-flop, a 5-V precision 1% reference, an undervoltage lockout control, and output circuitry (see Figure 1). Two totem-pole outputs are connected with common collectors and common emitters. These outputs are independent of device V_{CC} and device signal ground and provide good rise and fall time performance for power MOSFET control. The error amplifier has a common-mode voltage range from – 0.3 V to V_{CC} – 2 V. The dead-time control comparator has a fixed 0.1-V offset to prevent overlap of the outputs during push-pull operation. Synchronous multiple-supply operation can be achieved by connecting pin 6 to the reference output and providing a sawtooth input to pin 5. Circuit architecture prohibits the possibility of either output being pulsed twice during push-pull operation.

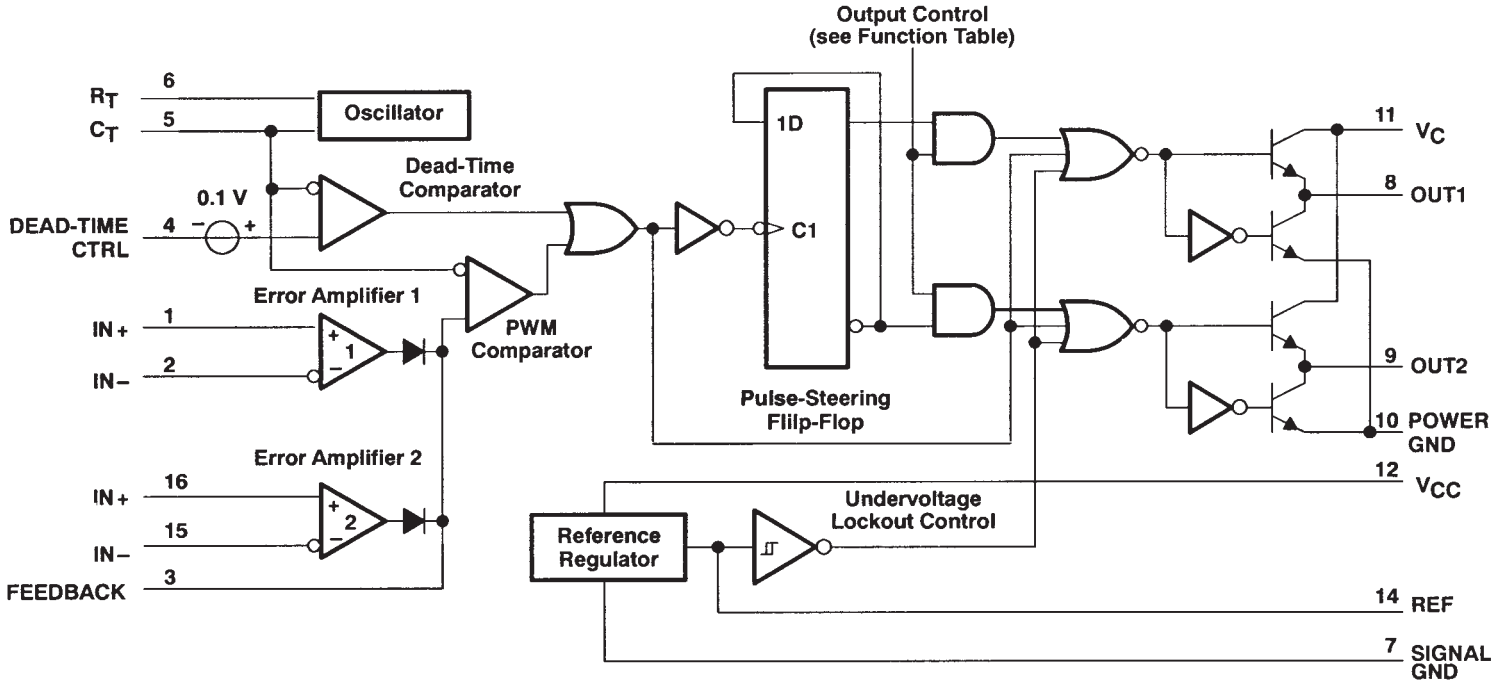


Figure 1. TL598 Block Diagram

TL598 Circuit Timing

Operation of the TL598 fixed-frequency pulse-width-modulation control circuit is illustrated by the timing diagram in Figure 2. Output pulse-width modulation is accomplished by comparison of the positive sawtooth waveform across C_T to either of two control signals. The NOR gates which drive the totem-pole outputs, OUT1 and OUT2, are enabled only when both the dead-time and PWM comparator outputs, ORed together, are in the low state. Also, the ORed low-state output is inverted and clocks a pulse-steering D-type flip-flop which alternately toggles OUT1 and OUT2 when the output-control input is high. When the output control input is grounded, the flip-flop outputs are interrupted by the two AND gates and outputs OUT1 and OUT2 operate in parallel.

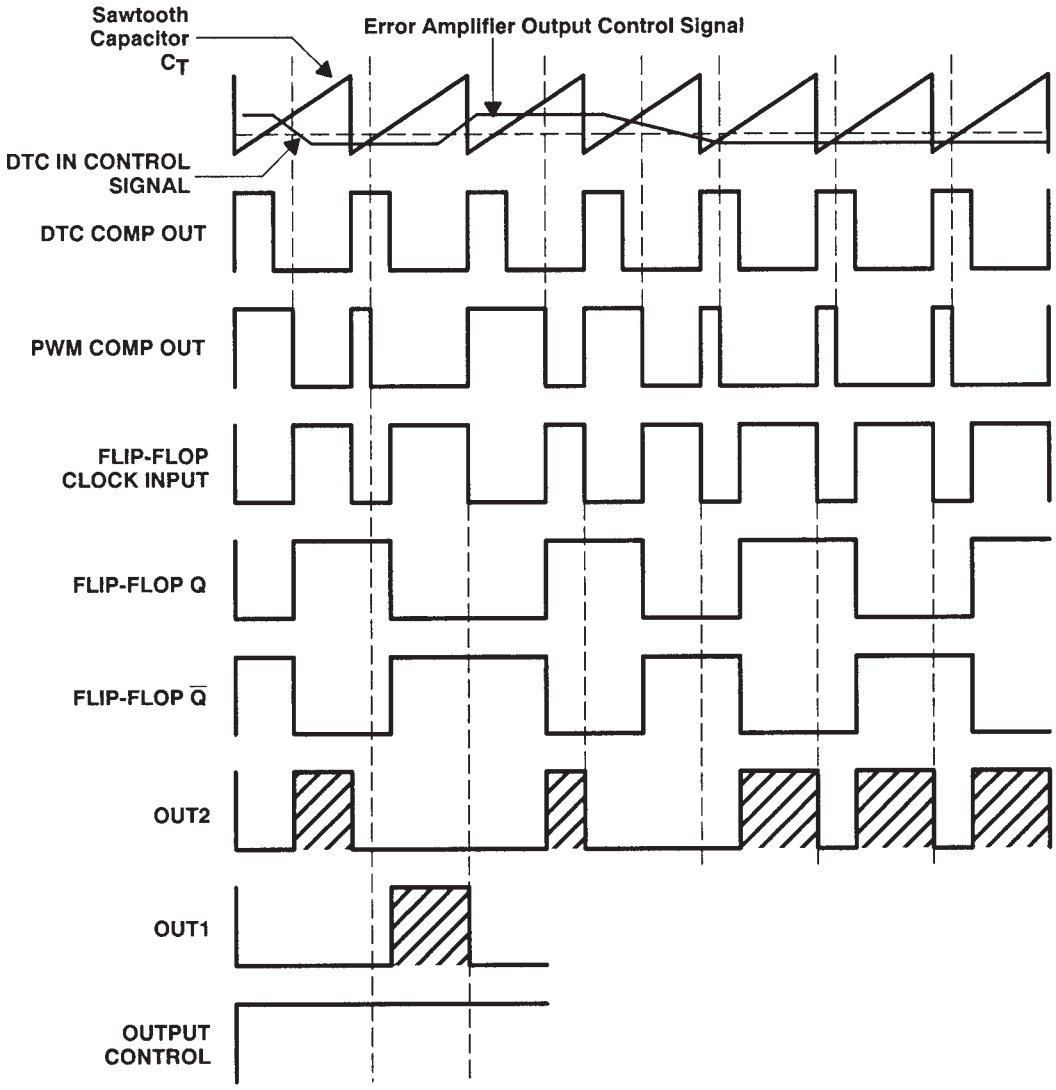


Figure 2. TL598 Circuit Timing Waveforms

Functional Description of the TL598 Circuit Operation

5-V Reference

The TL598 internal 5-V reference is shown in Figure 3. In addition to providing a stable reference, it establishes a stable supply from which the output control logic, pulse-steering flip-flop, oscillator dead-time-control comparator, and pulse-width-modulation comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain a thermal stability of less than 100-mV variation over the operating temperature range from 0°C to 70°C. Short-circuit protection is provided to protect the internal circuit from excessive load or short-circuit conditions. Designed primarily as an internal reference, 10 mA of load current is available for additional bias circuits. The reference is internally programmed to an initial accuracy of ±1% and will maintain a stability of less than 25-mV variation over an input voltage range from 7 V to 40 V. For input voltages less than 7 V, the regulator will saturate within 1 V of the input voltage and track it as shown in Figure 4.

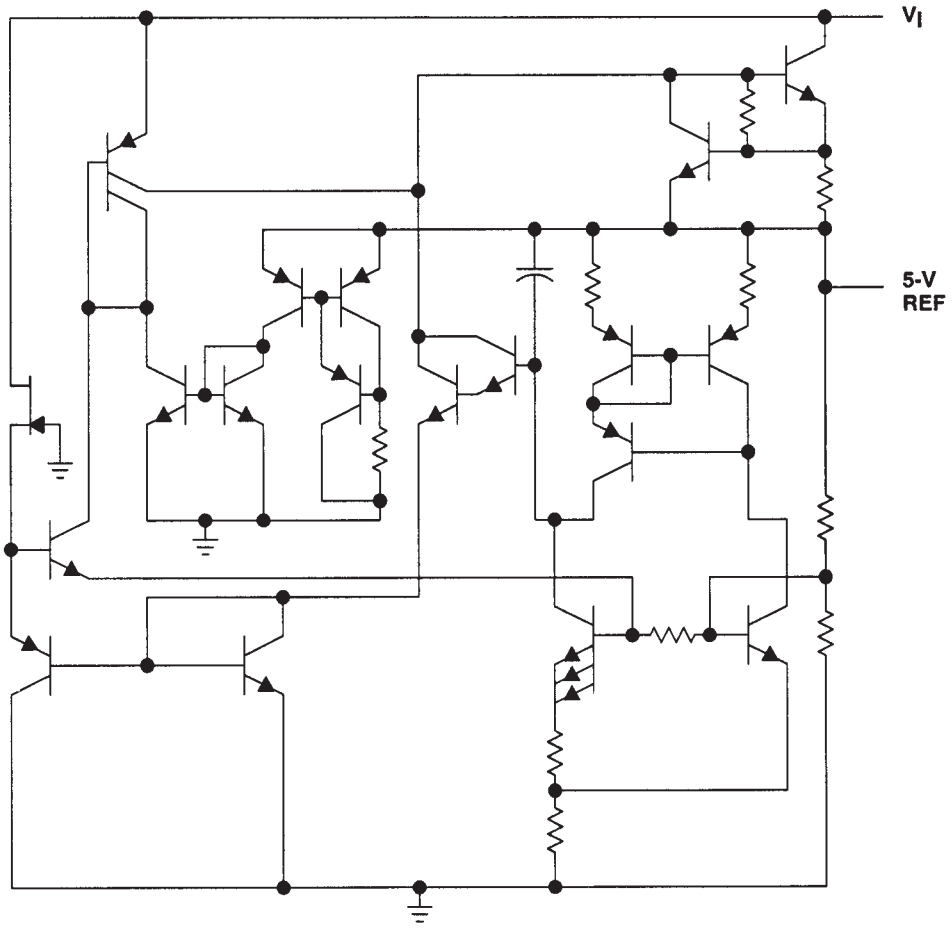


Figure 3. 5-V Reference Regulator Schematic

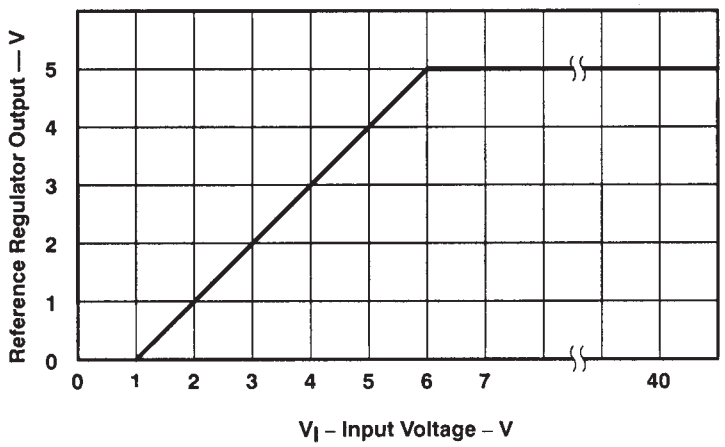


Figure 4. 5-V Reference Regulator Output vs Input Voltage

Oscillator

A schematic of the internal oscillator provided in the TL598 is shown in Figure 5. The oscillator provides a positive sawtooth waveform to the dead-time and pulse-width-modulation comparators for comparison with the various control signals. The frequency of the oscillator is programmed by selection of the timing components R_T and C_T. The oscillator charges the external timing capacitor C_T with a constant current which is determined by the external timing resistor R_T. This produces a linear-ramping voltage. When the voltage across the timing capacitor reaches 3 V, the oscillator circuit discharges the timing capacitor and the charging cycle is initiated again. The charging current is determined by:

$$I_{(charge)} = \frac{3\ V}{R_T}$$

The period of the sawtooth waveform is:

$$t_{clock} = \frac{3V \times C_T}{I_{(charge)}}$$

The frequency of the oscillator output then becomes:

$$f_o = \frac{1}{R_T C_T}$$

However, the oscillator frequency is equal to the output frequency only for single-ended applications. The output frequency for push-pull applications is one-half the oscillator frequency.

For single-ended applications: $f_o = \frac{1}{R_T C_T}$

For push-pull applications: $f_o = \frac{1}{2R_T C_T}$

The oscillator is programmable over a range from 1 kHz to 300 kHz. Practical values for R_T and C_T range from 1 kW to 500 kW and 470 pF to 10 mF, respectively. A plot of the oscillator frequency versus R_T and C_T is shown in Figure 6.

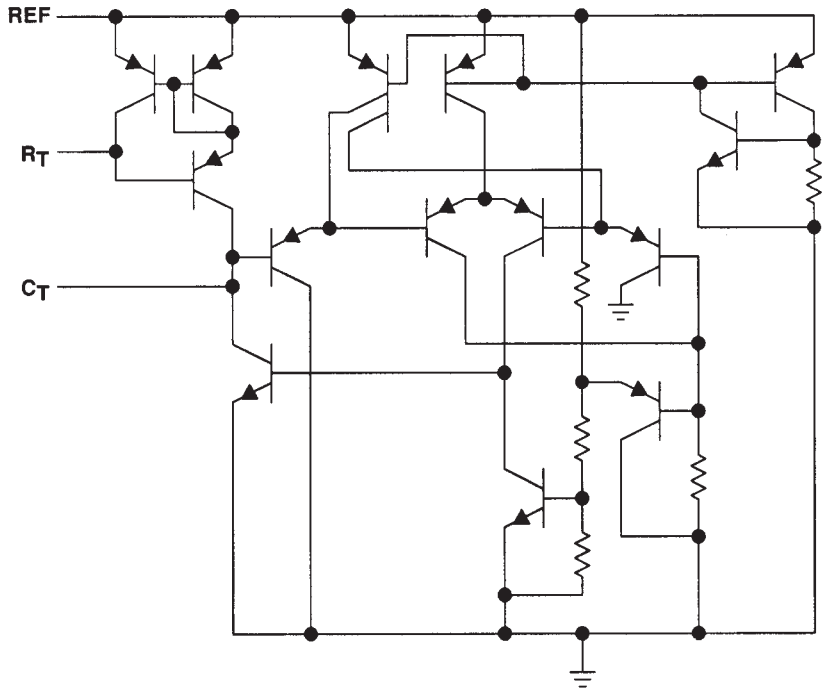
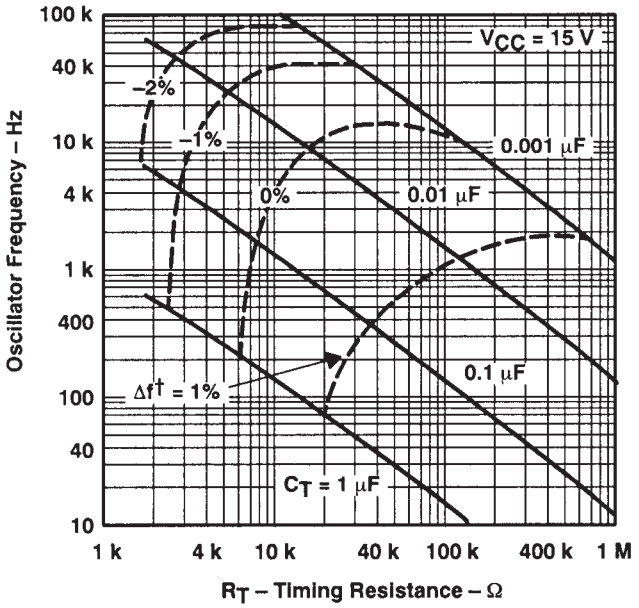


Figure 5. Oscillator Schematic



† Frequency variation (Δf) is the change in oscillator frequency that occurs over the full temperature range.

Figure 6. Oscillator Frequency vs Timing Resistance and Capacitance

Minimum Dead-Time for Oscillator Operation Above 150 kHz

At an operation frequency of 150 kHz, the period of the oscillator is 6.67 μs. The dead-time established by the internal offset of the dead-time-comparator (3% period) yields a blanking pulse of 200 ns with the dead-time-control input grounded (R23 = 0). This 200-ns period is the minimum blanking pulse acceptable to insure proper toggling of the pulse-steering flip-flop. For frequencies above 150 kHz, the 200-ns dead time or minimum blanking pulse must be provided by using the bias method shown in Figure 7. (See design example for details).

$$\frac{t_{clock}}{t_d} = \frac{3.3\ V}{0.1\ V + 5\ V \times \left(\frac{R23}{R23 + R22}\right)} = \frac{t_{clock}}{0.2\ \mu s}$$

therefore

$$\frac{R23}{R23 + R22} = \frac{\frac{3.3\ V \times 0.2\ \mu s}{t_{clock}} - 0.1\ V}{5\ V}$$

where

t_{clock} = clock period

t_d = dead time

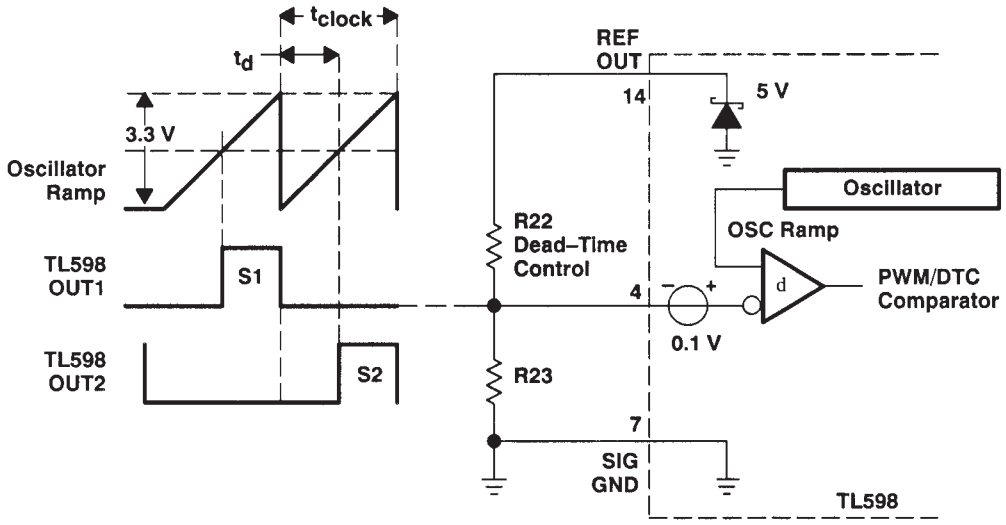


Figure 7. Dead-Time Generator

Dead-Time-Control and PWM Comparators

Although used as two separate comparators, the dead-time-control comparator and the PWM comparator use only one comparator circuit. A schematic of the single comparator circuit is shown in Figure 8. Since the two combined functions in the comparators are totally independent, each function can be discussed separately.

The dead-time control input provides control of the minimum dead (off) time. The output of the comparator for this function inhibits the switching transistors Q1 and Q2 when the voltage at its input (pin 4) is greater than the ramp voltage of the oscillator (the voltage across C_T at pin 5). Internal offset (110 mV) insures a minimum dead time of 3% with the dead-time-control input grounded. Additional dead time can be imposed by applying a bias voltage to the dead-time-control input. This provides a linear control of the dead time from its minimum 3% to 100% as the input bias voltage varies from 0 to 3.3 V, respectively. With full range control, it allows control of the output from external sources without disrupting the two error amplifiers. The dead-time-control input is a relatively high-impedance input (I_{IN} < 10 mA) and should be used where additional control of the output duty cycle is required. However, the input must be terminated for proper control. An open circuit is an undefined condition.

The C_T comparator also provides pulse-width-modulation control of the output pulse width. For this function, the ramp voltage across the timing capacitor C_T (pin 5) is compared to the control signal present at the output of the two error amplifiers (pin 3). The output pulse width varies from 97% of the period to zero as the voltage present at pin 3 varies from 0.5 V to 3.5 V, respectively.

The comparator is biased from the 5-V reference regulator. This provides isolation from the input supply for improved stability. The input of the comparator does not exhibit any hysteresis so caution should be observed to protect against false triggering about the threshold. The comparator exhibits a response time of 400 ns from either of the control signal inputs to the output transistors, with only 100-mV overdrive. This assures positive control of the output within a half cycle for operation within the recommended 300-kHz range.

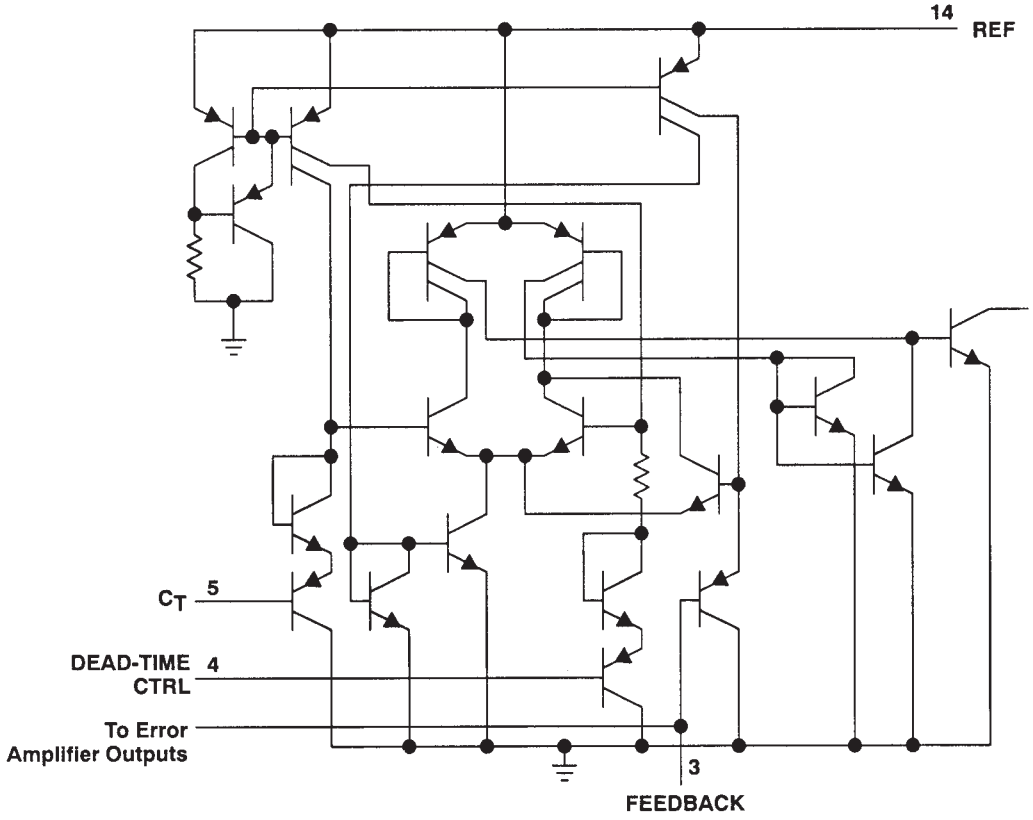


Figure 8. Dead-Time-Control and PWM Comparator

Error Amplifiers

The TL598 contains two high-gain error amplifiers. A schematic of one error amplifier circuit is shown in Figure 9. Both amplifiers receive their bias from the V_{IN} supply rail. This permits a common-mode input voltage range from $V_{IN} = -0.3$ V to -2 V. Both amplifiers operate as a single-ended single-supply amplifier, so each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With both outputs ORed together at the inverting input node of the PWM comparator, the amplifier demanding the minimum pulse out dominates. This node is biased low by a current sink to provide maximum pulse width out when both amplifiers are biased off. Figure 10 shows the output structure of the amplifier operating into the 300-μA current sink. Attention must be given to this node for biasing considerations in gain-control and external-control interface circuits. Since this point (amplifier output) is biased low only through a current sink (I_{SINK} = 300 μA), bias currents required into this node by external circuitry must not exceed the capability of the current sink. If this happens, the maximum output pulse will be limited. Figure 11 illustrates the proper-biasing techniques for feedback gain control to assure that the 300-μA sink-current capability of the output structure is not exceeded.

A plot of the transfer characteristics of the amplifiers is shown in Figure 12. This illustrates the linear-gain characteristics of the amplifiers over the active input range of the PWM comparator (0.5 V to 3.5 V). This is important for overall circuit stability. The open-loop gain of the amplifiers for output voltages from 0.5 V to 3.5 V is 60 dB. A Bode plot of the amplifiers gain characteristics is shown in Figure 13. Both amplifiers exhibit a response time of approximately 400 ns from their inputs to their outputs. The

amplifier's ability to respond to an increasing load demand can be severely degraded by capacitive loads on pin 3 since the amplifiers employ active pullup only. Therefore, caution should be taken to minimize capacitive loading of the amplifiers.

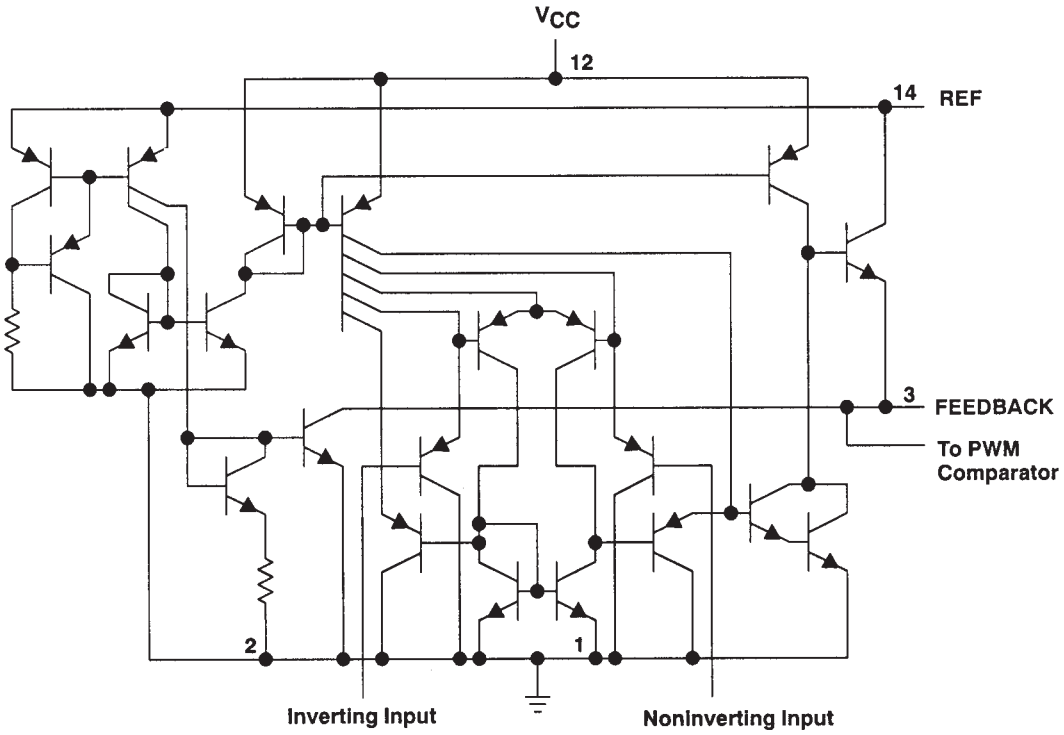


Figure 9. Error Amplifier

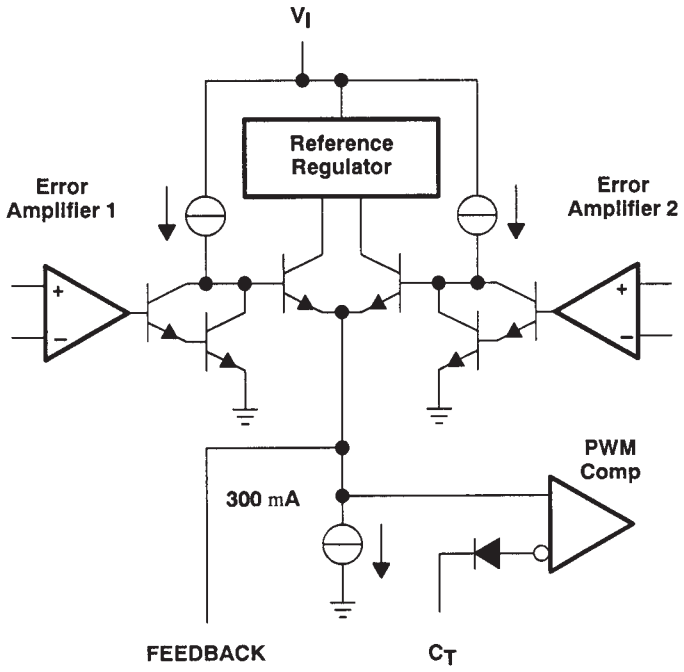


Figure 10. MUX Structure of Amplifiers

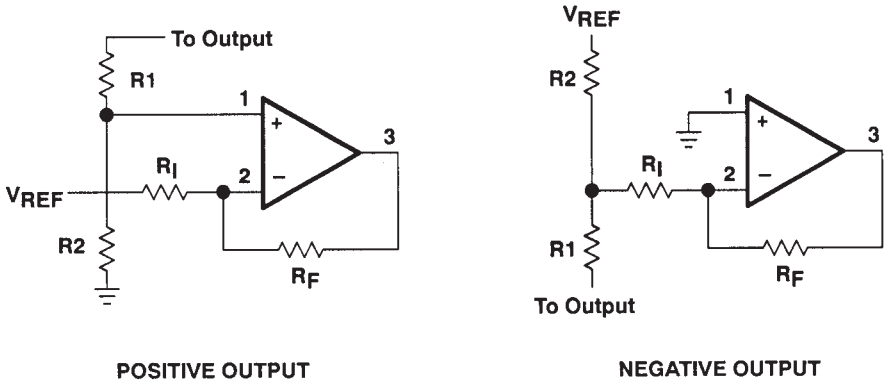


Figure 11. Error Amplifier Bias Circuits for Controlled Gain Applications

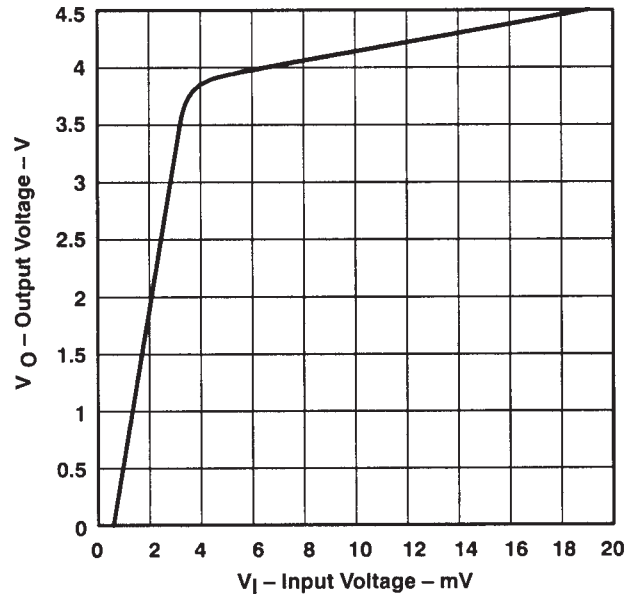


Figure 12. Amplifier Transfer Characteristics

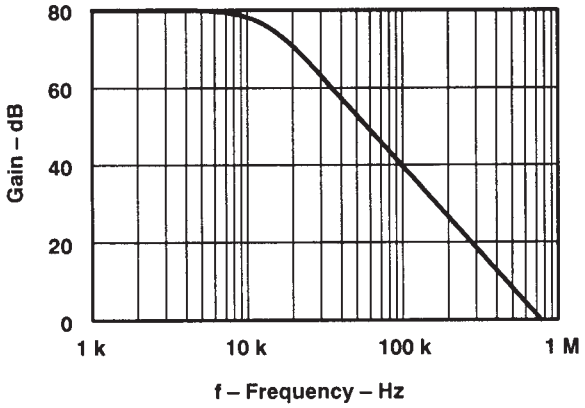


Figure 13. Amplifier Bode Plot

Output Control Logic

The output control logic is structured to provide added versatility through external control. Designed for either push-pull or single-ended applications, circuit performance can be optimized by selection of the proper conditions applied to the various control inputs. The output-control input determines whether the output transistors operates in parallel or push-pull. The output-control input is the supply source for the pulse-steering flip-flop as shown in Figure 14. This input is an asynchronous input. It has direct control over the output and is independent of the oscillator or pulse-steering flip-flop. It is intended to be a fixed condition defined by the application. For parallel operation, the output-control input must be grounded. This disables the pulse-steering flip-flop and inhibits it outputs. In this mode, the pulses seen at the output of the dead-time-control/pulse-width-modulation comparator are transmitted by both output transistors in parallel. For push-pull operation, the output-control input must be connected to the internal 5-V reference regulator. Under this condition, each of the output transistors is alternately enabled by the pulse-steering flip-flop.

Pulse-Steering Flip-Flop

The pulse-steering flip-flop is a positive edge-triggered D-type flip-flop that changes state synchronously with the rising edge of the comparator output. A schematic of the pulse-steering flip-flop is shown in Figure 15. The guaranteed dead time provides blanking during this period to insure against the possibility of having both outputs on simultaneously during the transition of the pulse-steering flip-flop outputs. The duration of the blanking pulse also has to be sufficient to allow proper steering of the pulse-steering flip-flop. The minimum trigger pulse is 200 ns. If the internal 3% dead time is employed, the maximum frequency of operation for the internal oscillator is 150 kHz. For operation above this frequency, see functional description of the TL598 circuit operation (minimum dead time).

Since the flip-flop receives its trigger from the output of the comparator, the output always operates push-pull. This prevents double pulsing of either output in light-load or transient-load situations. The flip-flop will not change state unless an output pulse occurred during the previous oscillator period.

Output Transistors

There are two 200-mA totem-pole outputs available on the TL598. The output structure is illustrated in Figure 16. Each output is capable of sinking or sourcing up to 200 mA of current. The transistors will exhibit a saturation voltage of less than 2 V in the source configuration and less than 2 V in the sink configuration. The outputs are protected against excessive power dissipation to prevent damage but do not employ sufficient current limiting to allow them to be operated as current-source outputs.

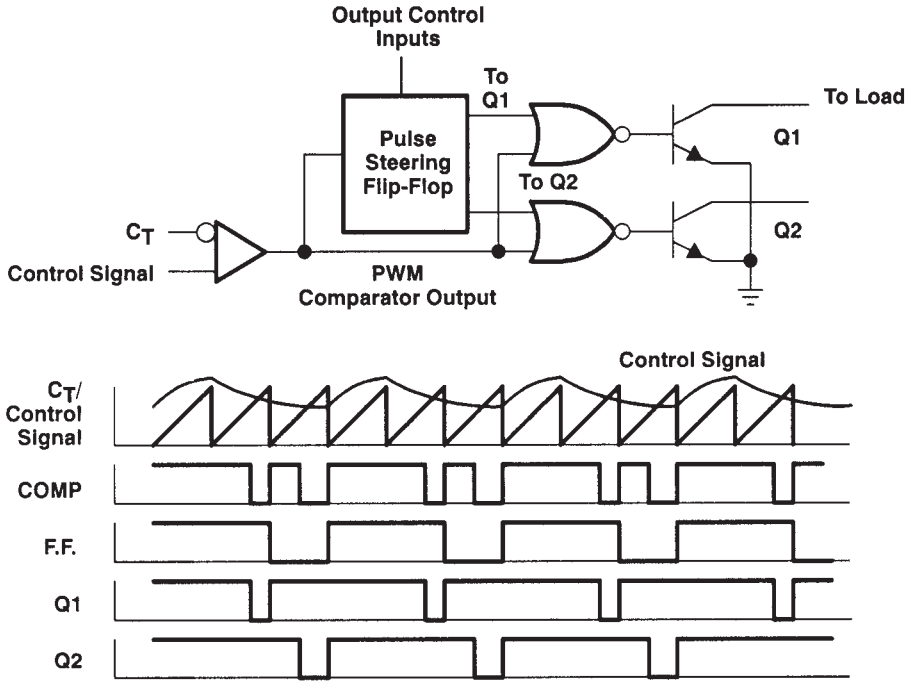
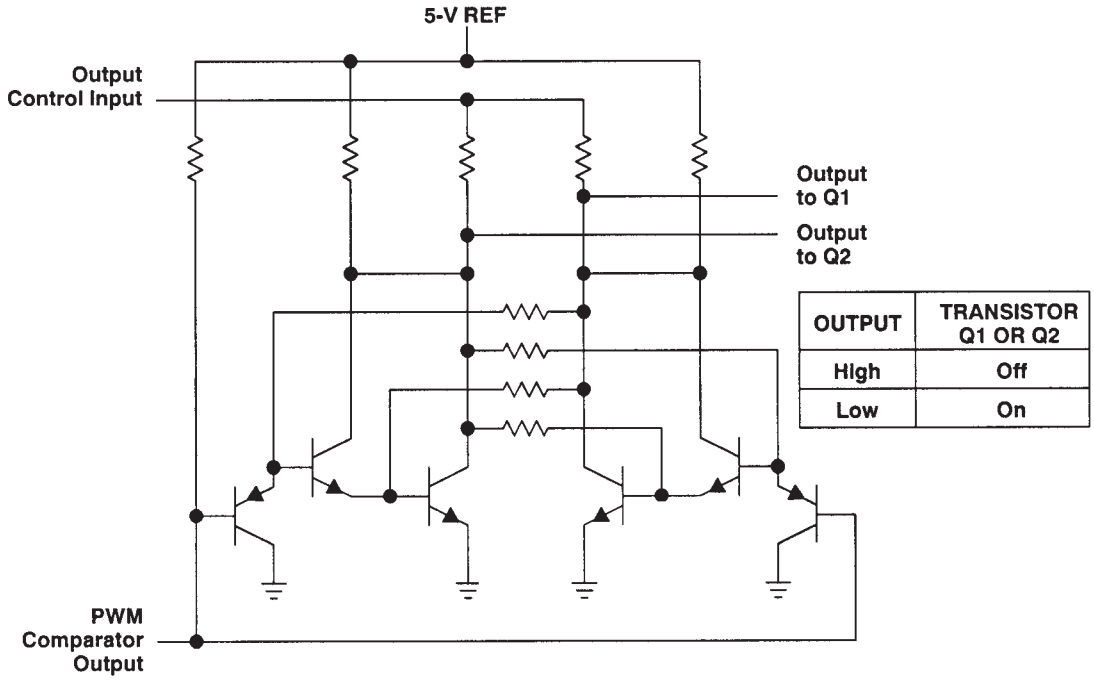


Figure 14. Output Steering Circuit



OUTPUT	TRANSISTOR Q1 OR Q2
High	Off
Low	On

Figure 15. Pulse-Steering Flip-Flop

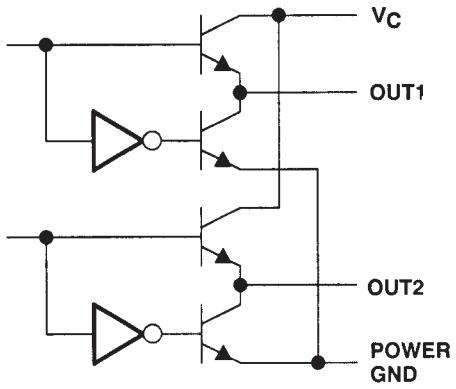


Figure 16. Totem-Pole Output Circuits

DC-to-DC Converter Design Example Using the TL598

Push-Pull Converter

The design example is for a 50-W dc-to-dc push-pull converter operating from a 48-V telephone central-office supply. The nominal voltage is 48 V and the design is for a minimum voltage of 42 V and a maximum voltage of 56 V. The operating frequency is 100 kHz. Additional design requirements are:

Regulated Output Power:

5 V + 0.5% at 10 A

Ripple:

Shall be less than 125-mV peak-to-peak

Efficiency:

75% minimum at full load

Protection Circuits:

Both the input and output shall be overvoltage and undervoltage protected and the output shall be short-circuit protected. Also signals of undefined operation between V_O (2.2 V – 4.2 V) and between V_O (2.2 V – 4.55 V) shall be provided.

Block Diagram and Waveforms

A simplified circuit of the push-pull converter power section is shown as Figure 17 while the waveforms of Figure 18 illustrate the voltage and current characteristics of the power section.

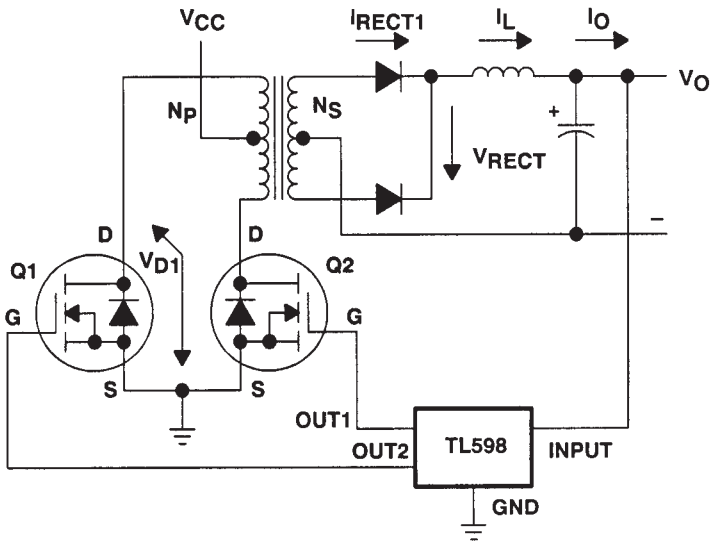


Figure 17. Push-Pull Converter Power Section

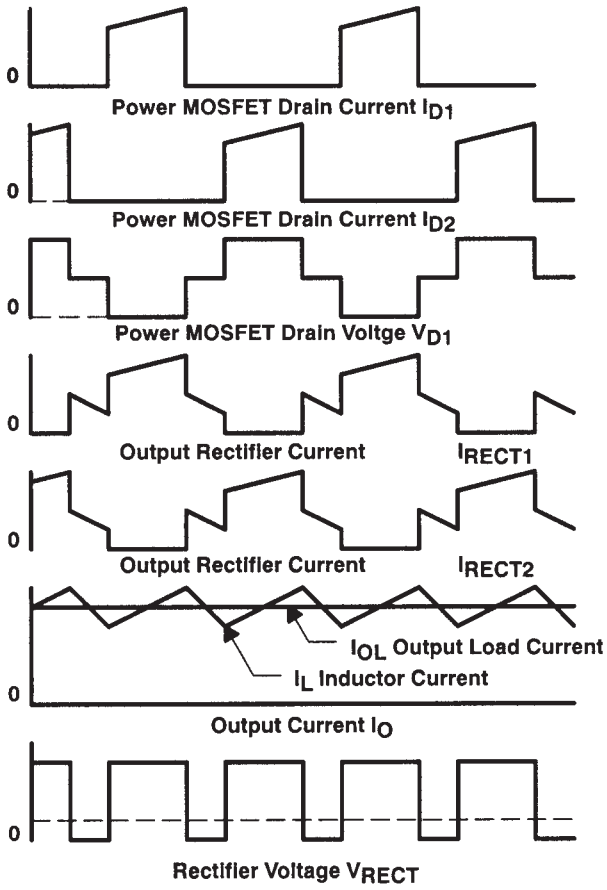


Figure 18. Push-Pull Converter Waveforms

Transformer and Power Switches

Equation (1) is used to estimate the transformer maximum turns ratio:

$$N = \frac{N_P}{N_S} = \frac{V_P}{V_S} = \frac{\delta \times V_{I(MIN)}}{V_O + V_D} \quad (1)$$

where

N_P = number of turns on primary
N_S = number of turns on secondary
N = turns ratio
d = duty cycle (85% assumed)
V_I = input voltage (42 V MIN) (56 V MAX)
V_O = regulated output voltage = 5 V
V_D = rectifier on voltage = 1 V

$$N = \frac{(0.85) \times (42\ V)}{5\ V + 1\ V} = 5.95 \text{ MAX turns ratio}$$

The AIE magnetics transformer (part number 320-0616) has a turns ratio (N_P:N_S) of 10:2, output power of 51 W, switching frequency of 1.5 MHz, output current of 10 A, and is selected for the application.

Based on the 320-0616 transformer with a turns ratio N of 5, the converter duty cycle, δ, is calculated for minimum and maximum input voltages:

For $V_{I(MIN)} = 42$ V,

$$\delta = \frac{(V_O + V_D)\,(N)}{V_{I(MIN)}} = \frac{(5 + 1)\,(5)}{42} = 0.71$$

For $V_{I(MAX)} = 56$ V,

$$\delta = \frac{(V_O + V_D)\,(N)}{V_{I(MAX)}} = \frac{(5 + 1)\,(5)}{56} = 0.53$$

The total power provided to the transformer secondary is

$$P_{(SEC)} = 10\text{ A} \times (5\text{ V} + 1\text{ V}) = 60\text{ W};$$

$$P_{(SEC)}\text{ Avg} = 60\text{ W} \times \delta = 60\text{ W} \times 0.85 = 51\text{ W}$$

Assuming the converter transformer efficiency is 95%, the transformer input power on the primary is

$$P_{(PRI)} = \frac{60\text{ W}}{0.95} = 63.2\text{ W}$$

Under low-input line-voltage conditions, the maximum duty cycle is 0.71 and the voltage applied to the transformer primary is 42 V. The peak primary current is

$$I_{pk(Q1)} = I_{pk(Q2)} = \frac{63.2\text{ W}}{0.71 \times 42\text{ V}} = 1.79\text{ A}$$

The actual peak current is estimated to be about 10% higher due to magnetizing current in the converter transformer, or about 2 A peak. The peak switch voltage is estimated to be approximately

$$V_{pk(Q1)} = V_{pk(Q2)} = 1.3 \times (2 \times V_I) = 1.3 \times (2 \times 56) = 145\text{ V}$$

Type IRF620 N-channel power MOSFETs were selected for the power switches based on their 200-V V_{DS} and 5-A I_D maximum ratings.

Output Filter

The output inductor is selected to limit the ripple current that the output capacitors must filter. The equation (2) below is used to calculate the required inductance, L, after the inductor ripple current Δi_L is defined. Inductor ripple current equal to 10% of the maximum output current, I_O, is used in this design.

$$L = \frac{(V_O + V_D)\,(1 - \delta)\,(t_{clock})}{\Delta i_L} \qquad (2)$$

where

δ = duty cycle = 53%
V_I = 56 V Max
V_O = output voltage = 5 V
V_D = output rectifier on voltage = 1 V
Δi_L = inductor peak-to-peak ripple current (10% of 10 A) = 1 A
t_{clock} = clock period = 5 μs

$$L = \frac{(5\ V + 1\ V)\ (1 - 0.530)\ 5\ \mu s}{1\ A} = 14.1\ \mu H$$

A 16-μH inductor is chosen to satisfy the above equation. Since the filter inductance has been chosen, the output capacitor can be selected to meet the ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. If good filtering is to be provided, the ripple frequency must be far below those frequencies at which the series inductance becomes important. This means the two components of interest are the capacitance and the series resistance, RC. To estimate the equivalent-series-resistance (ESR) ripple voltage, $\Delta V_{O(ESR)}$, it is assumed that all the ripple current in the inductor, Δi_L, flows through the output capacitance.

$$\Delta V_{O(ESR)} = \Delta i_L \times R_S$$

where

$\Delta V_{O(ESR)}$ = peak-to-peak ripple voltage due to ESR
Δi_L = peak-to-peak ripple current
R_S = capacitor equivalent-series-resistance (Ω)

The peak-to-peak ripple voltage due to capacitance is:

$$V_{O(C)} = \frac{\Delta i_L \times t_{clock}}{8 \times C}$$

where

t_{clock} = clock period = 5 μs

the maximum capacitor ESR is then

$$R_S < \frac{0.125\ V}{1A} = 0.125\ \Omega.$$

The Sprague 674D158H012HE5A, 1500-μF, 12-V capacitor is selected because it has a maximum ESR of 0.055 Ω and a maximum ripple current of 3.3 A. The ripple voltage due to capacitance is:

$$V_{O(C)} = \frac{(1\ A) \times (5 \times 10^{-6}\ s)}{8 \times (1500 \times 10^{-6}\ F)} = 0.00042\ V$$

which is negligible.

Oscillator

The TL598 oscillator frequency is programmed with an external capacitor C_T and an external resistor R_T connected to pins 5 and 6. The oscillator clock frequency, f_{clock}, must be set at 200 kHz for the converter to operate at the specified f_{op} = 100 kHz.

$$f_{op} = \frac{1}{2\ R_T\ C_T}$$

Choose C_T = 0.001 μF and calculate R_T.

$$R_T = \frac{1}{2 \times f_{op} \times C_T}$$

$$R_T = \frac{1}{2 \times (100 \times 10^3) \times (0.001 \times 10^{-6})}$$

$$R_T = 5 \times 10^3\ \Omega$$

Dead-Time Circuitry

The converter duty cycle (see Figure 19) is defined as:

$$\delta = \frac{(t_w \times 2) \times 100\%}{t_p}$$

This duty cycle must not be limited to less than 71.0% or the supply may not be able to output rated voltage at low-input line voltage. It is also important to limit the maximum duty cycle to 93% to allow the IRF620 power MOSFET switches a switching time of 0.2 μs (see Transformer and Power Switches section). An 85% duty-cycle design is selected. By choosing R23 = 1 kΩ, R22 is calculated to be 13 kΩ using the equation below:

$$\frac{t_{clock}}{t_d} = \frac{3\ V}{0.1\ V + 5\ V\left(\frac{R23}{R23 + R22}\right)}$$

$$R22 = R23\left[\left(\frac{5\ V}{\frac{3\ V \times t_d}{t_{clock}} - 0.1\ V}\right)^{-1}\right]$$

$$R22 = 1 \times 10^3\left[\left(\frac{5}{\frac{3 \times .75 \times 10^{-6}}{5 \times 10^{-6}} - 0.1}\right)^{-1}\right]$$

$$R22 = 13\ k\Omega$$

where

t_{clock} = 5 μs =clock period,
t_d = 0.75 μs = dead time,
R23 = 1 kΩ

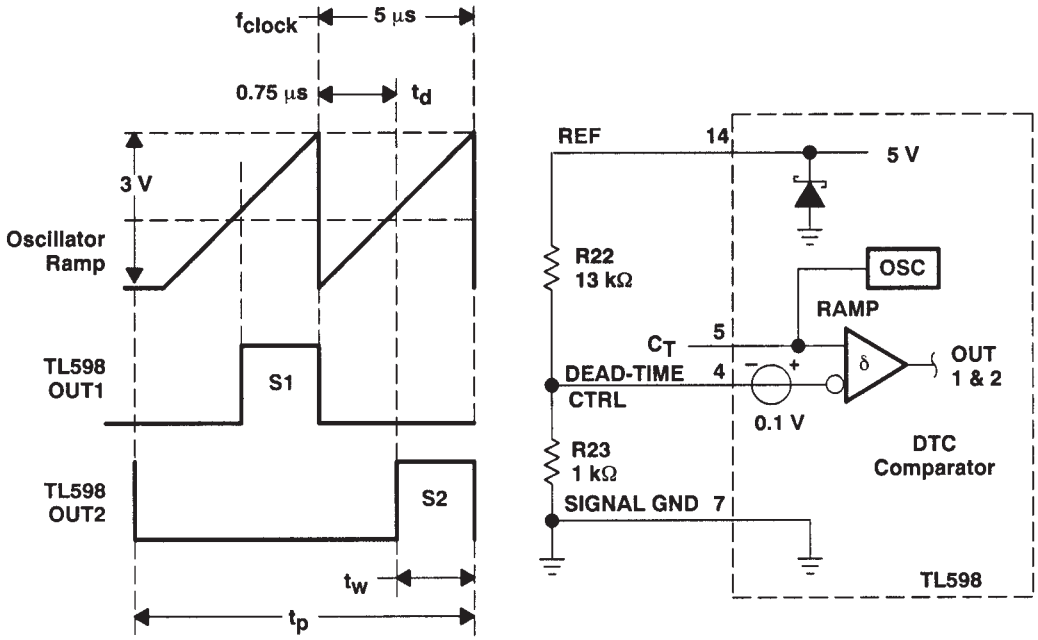


Figure 19. DTC Comparator Circuit and Waveforms

Soft-Start Circuitry

It is necessary to reduce the surge due to the charge on the output capacitors at power startup to reduce stress on the IRF620 power MOSFET switches. By applying a negative-slope waveform to pin 4 of the dead-time comparator, the soft-start characteristic is achieved, allowing the pulse duration at the output stage to increase slowly (see Figure 20).

The soft-start timing capacitor is selected to provide a time constant τ, which is approximately one-third the desired output rise time t_r (50 ms), and is equal to:

$$\tau = \frac{1}{3}(t_r) = \frac{(C15)(R22 \times R23)}{(R22 + R23)} \text{ or}$$

$$C15 = \frac{1}{3}(t_r)\left(\frac{R22 + R23}{R22 \times R23}\right)$$

C15 is calculated to be 18 μF

where

t_r = 5 ms
R22 = 13 kΩ
R23 = 1 kΩ

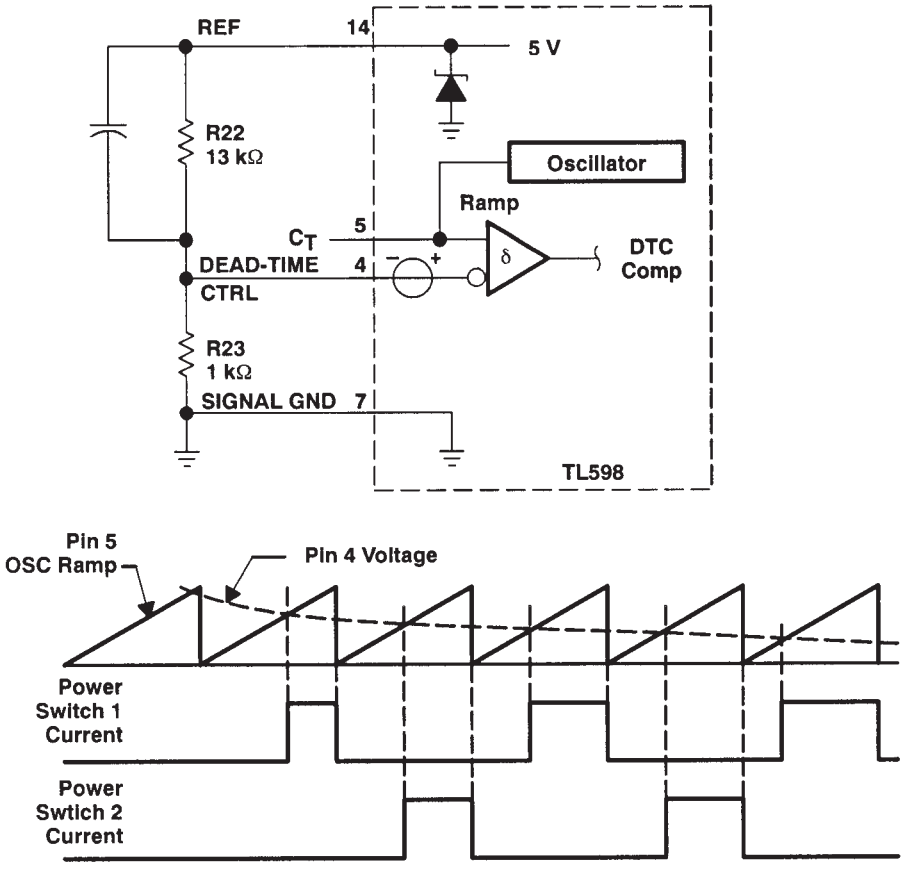


Figure 20. Soft-Start Circuit and Waveforms

Overcurrent Protection

A current-sense resistor, R4, is placed in the primary side of the power transformer, T3, so that it will be responsive to core saturation as well as provide overcurrent limiting by use of the TL598 dead-time control input (Figure 21).

The load-fault primary current, I_p, chosen for the design is 2 A based on the peak primary-current calculation in the transformer and power switches section. Therefore, at the 2-A fault condition, an output voltage, V_O, of approximately 1 V will be produced across R4. At V_O = 1 V, the voltage-divider network consisting of R30 and R31 is designed to turn on Q6 which turns on Q5. The turned-on Q5 applies the 5-V reference voltage to pin 4 of the dead-time comparator. The reference voltage on pin 4 causes the output drive to be terminated and also toggles the pulse-steering flip-flop to the other output drive prior to the completion of the oscillator period. However, both output drives are inhibited because C15 is discharged through the turned-on Q5. This action causes a voltage to remain on pin 4 until C15 can charge through R23 according to the normal soft-start mode. This mode is described in the dead-time circuitry section.

Input-Voltage Overvoltage Protection

The programmable TL431 (see Figure 22) precision reference is used to sense a sample of the input line voltage developed across the R50-R51 voltage divider. When the voltage across the divider reaches approximately 1.86 V, the TL431 conducts and turns on Q5. The turned-on Q5 applies the 5-V reference to pin 4 of the dead-time comparator which causes both TL598 output drives to be terminated.

Since the converter has a specified input-voltage range of 42 to 56 V, the R50-R51 divider was selected for an overvoltage trip point of 60.6 V.

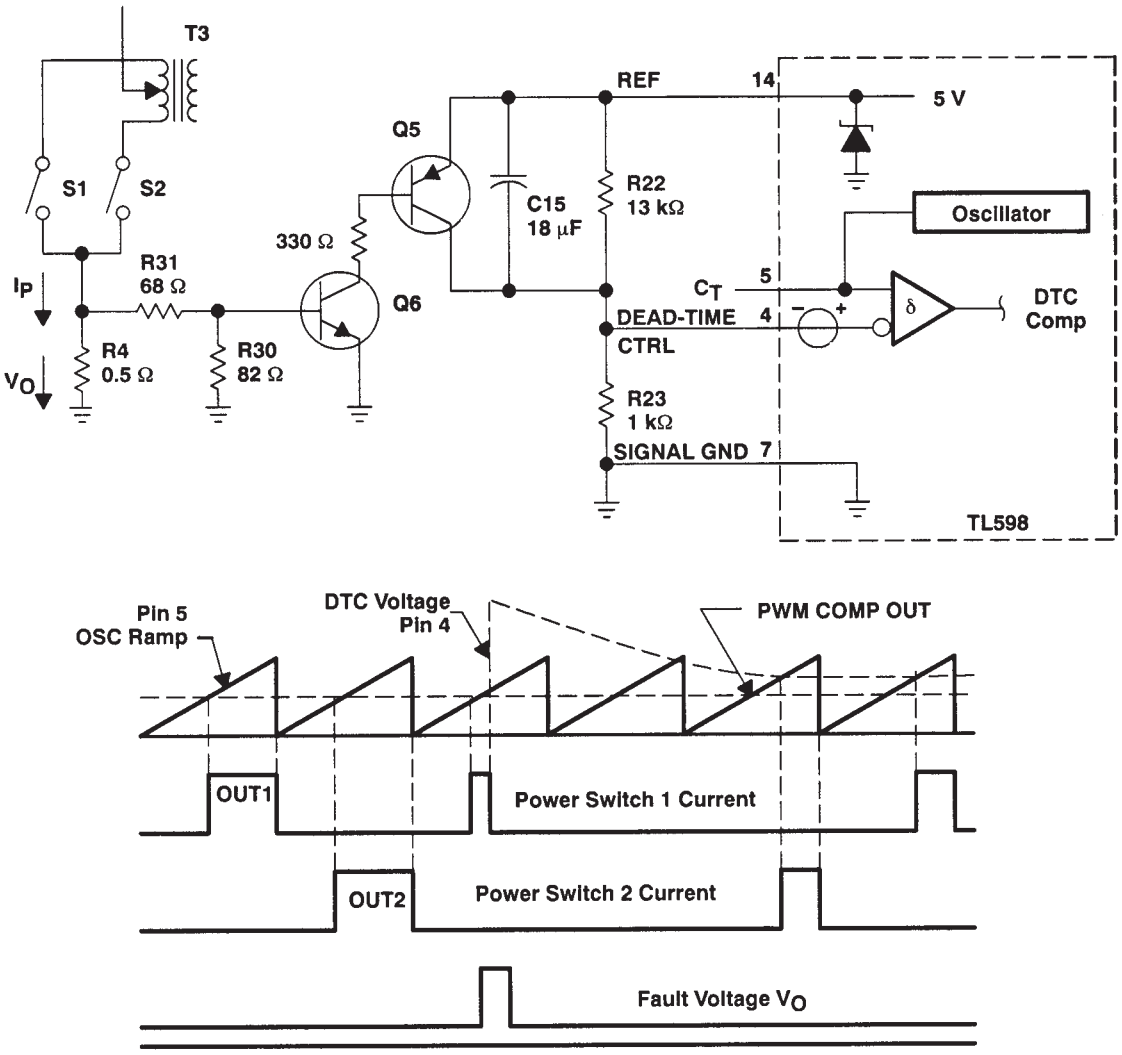


Figure 21. Overcurrent Protection Circuit and Waveforms

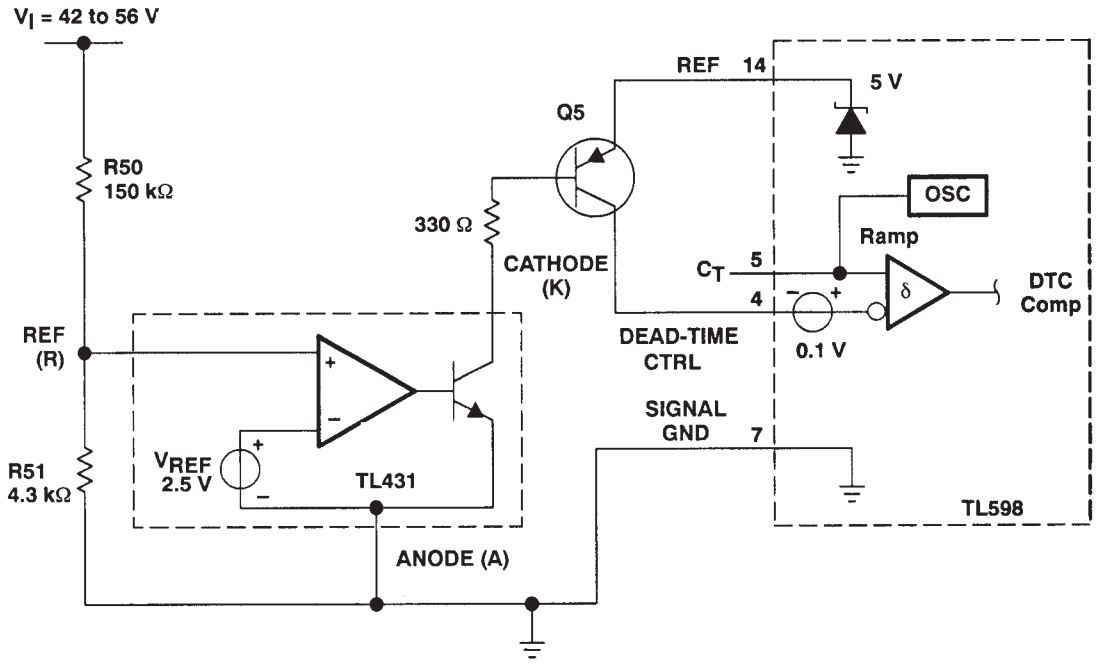


Figure 22. Overvoltage Protection Circuit

Error-Amplifier Bias and Compensation Network

The TL598 error amplifier (see Figure 23) compares the 5-V output to the 5-V voltage reference and adjusts the pulse-width modulator to maintain the proper output. Connected to the error-amplifiers feedback terminal is a compensation network which shapes the frequency response of the amplifier so that the power supply system is stable over the range of line and load variations. To ensure that this system is stable, the design objective is for a 60° phase margin at system crossover frequency, f_{CRO}, while f_{CRO} is selected as one-fifth of the 100-kHz switching frequency or 20 kHz.

The pulse-width modulator converts an error voltage into a drive pulse. The modulator used in the TL598 is a comparator with a triangular wave applied to one input and the error voltage, V_{ERROR}, applied to the other input. The drive-command duration, t_{on}, is equal to the time the sawtooth exceeds the error voltage. The drive pulse width changes from maximum, t_{clock}, to minimum as the error signal changes from the minimum ramp value to its maximum of 3 V.

Therefore

$$V_{ERROR} = \left(1 - \frac{t_{on}}{t_{clock}}\right) \times 3\ V = (1 - d) \times 3\ V$$

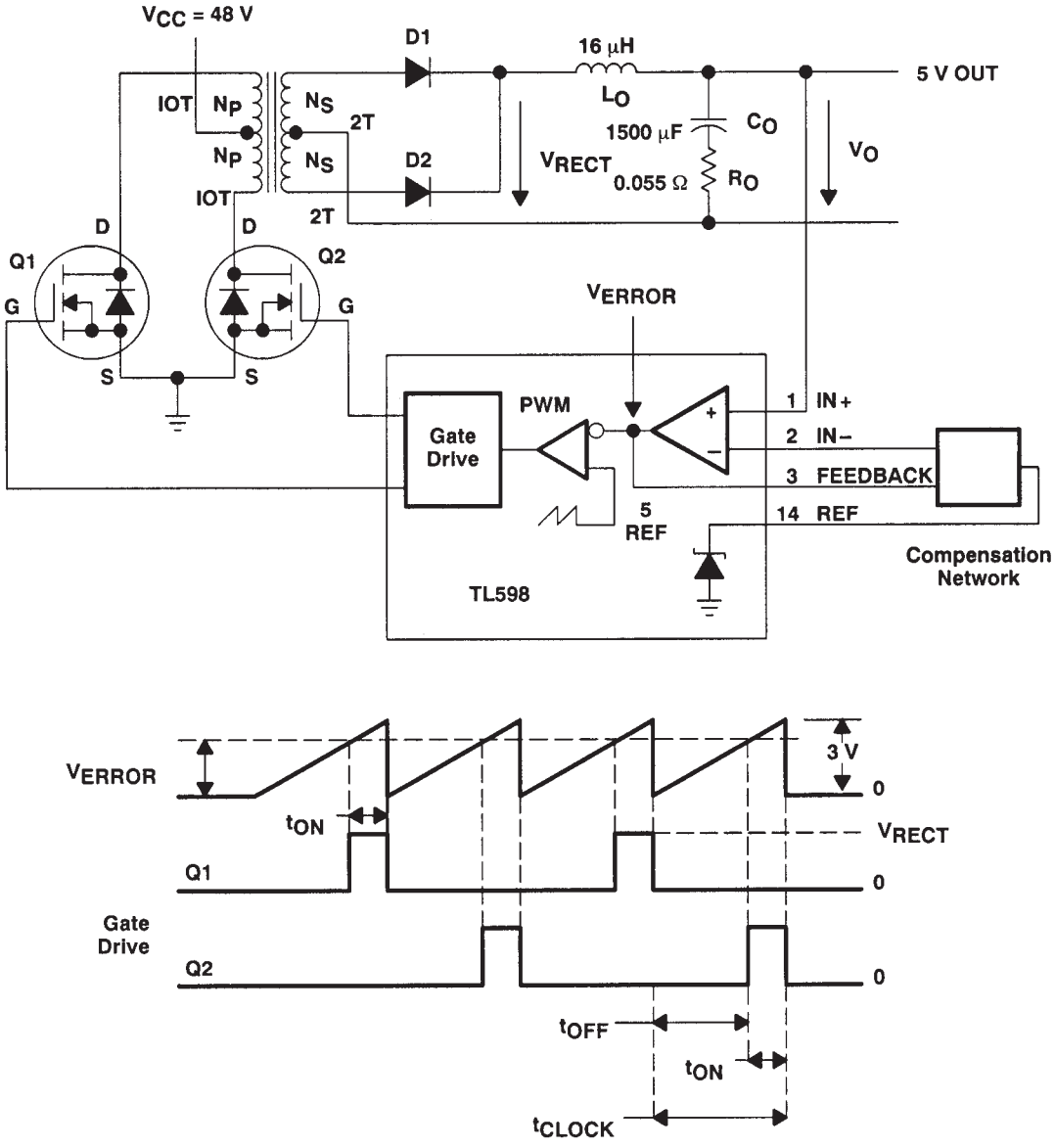


Figure 23. Error Amplifier and Compensation Circuits With Waveforms

Gain and Phase Calculations

The dc gain of the power modulator is defined as

$$G_{PM} = \frac{V_O}{V_{ERROR}}$$

and the output voltage, V_O, is defined as

$$V_O = \left(d \times \frac{V_{CC}}{N} \right) - V_D$$

where

V_{CC} = 48 V (nominal design) = input voltage
N = 5 = transformer turns ratio
V_D = 1 V = rectifier-on voltage
d = 0.625 = power converter duty cycle for V_O = 5 V

therefore from equation (5)

$$V_{ERROR} = (1 - \delta) \times 3\ V = (1 - 0.625) \times 3\ V = 1.125\ V$$

and the dc gain of the power modulator, G_{PM}, is:

$$G_{PM} = \frac{V_O}{V_{ERROR}} = \frac{5\ V}{1.125\ V} = 4.44$$

The calculations for output filter gain and phase lag are shown using a graphical solution. The corner frequency of the output filter (slope = – 2) is defined as :

$$f_{LC}\ (\text{corner}) = \frac{1}{2 \times \pi \times \sqrt{L_O \times C_O}}$$

The frequency at the start of the –1 slope (filter capacitor) is defined as:

$$f_{ESR}\ (\text{zero}) = \frac{1}{2 \times \pi \times R_O \times C_O}$$

where

R_O = 0.055 W
L_O = 16 mH
C_O = 1500 mF

Therefore

f_{LC}(corner) = 1027 Hz
f_{ESR} (zero) = 1929 Hz

Using the calculated values of G_{PM}, f_{LC} (corner), and f_{ESR} (zero), the power-modulator/output-filter gain is plotted versus frequency on reactance frequency graph paper (see Figure 24).

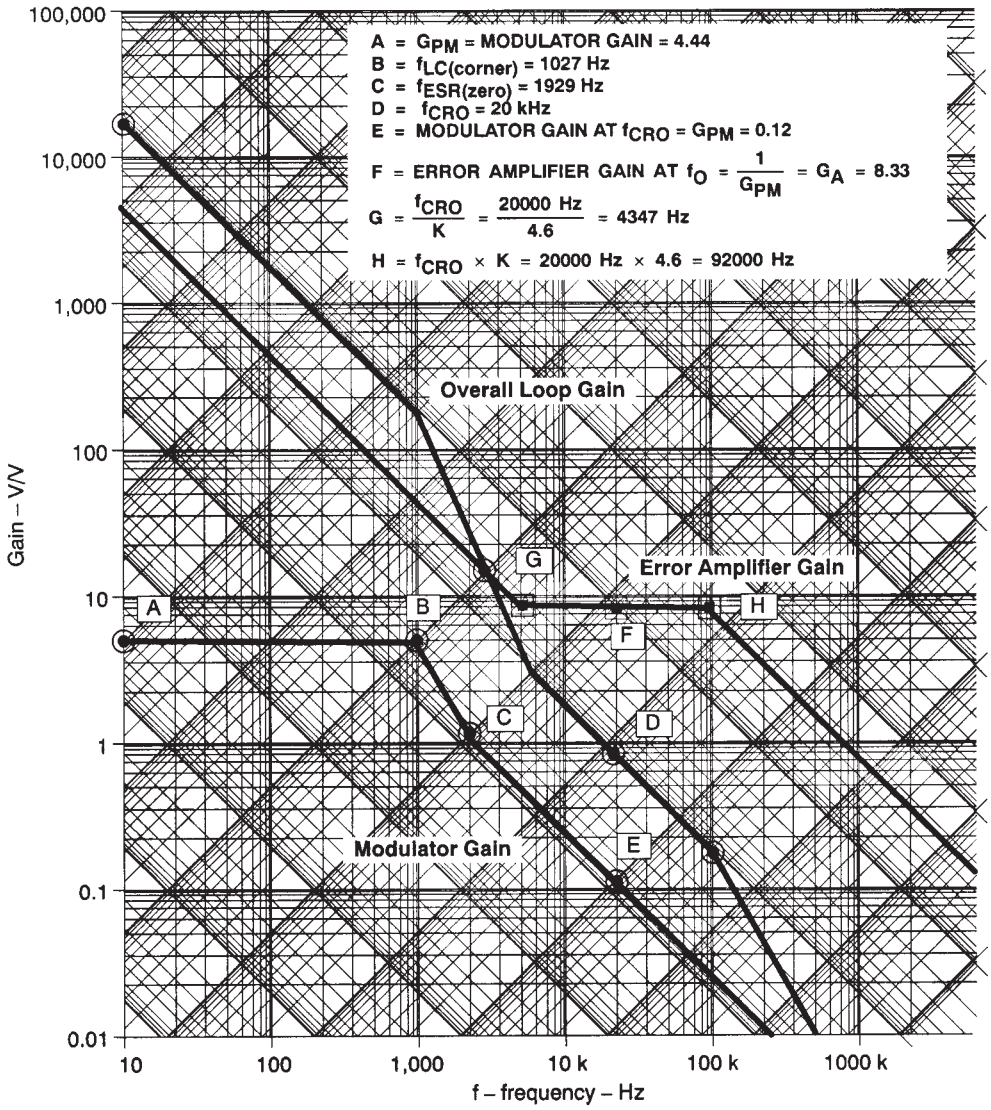


Figure 24. Power Modulator/Output Filter Gain vs Frequency

The phase lag of the LC output filter at the 20-kHz crossover frequency, f_{CO}, is defined as:

$$\theta_{LC} = 180^\circ - \arctan\left(\frac{f_{CRO}}{f_{ESR\ (zero)}}\right)$$

$$\theta_{LC} = 180^\circ - \arctan\left(\frac{20{,}000\ Hz}{1929\ Hz}\right) = 95.5^\circ$$

The error amplifier and loop compensation network design methods used in this report are based on analysis techniques described by Dean Venable (see Reference 1). The type-2 amplifier design (see Figure 25) was selected for the error amplifier since only 65.5° of boost is needed for the amplifier to provide the design objective of 60° phase margin at the 20-kHz crossover frequency. The phase angles in the design are:

$\theta_{FB} = 180^\circ$ from negative feedback

$\theta = 90^\circ$ from amplifier pole at origin

$\theta_{LC} = 95.5^\circ$ from power modulator LC filter

$\theta_T = 365.5^\circ$ total phase shift

θ_B (boost) = $\theta_T - (360^\circ -$ design phase margin)

θ_B (boost) = $365.5^\circ - (360^\circ - 60^\circ) = 65.5^\circ$

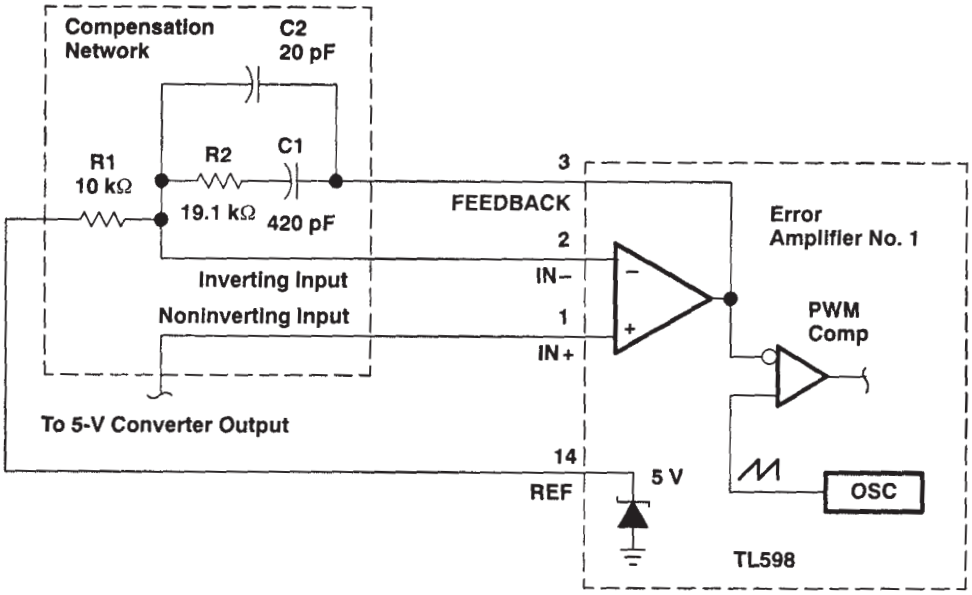


Figure 25. Error Amplifier and Loop Compensation Circuits

The following equations apply to type-2 amplifiers:

$$K = \tan\left(\frac{\theta_B}{2} + 45^\circ\right) = 4.6$$

$$C2 = \frac{1}{2 \times \pi \times f_{CRO} \times G_A \times K \times R1} = 20.7 \text{ pF}$$

$$C1 = C2 \times (K^2 - 1) = 417 \text{ pF}$$

$$R2 = \frac{K}{2 \times \pi \times f_{CRO} \times C1} = 19,093\ \Omega$$

where

$R1 = 10$ kΩ

$f_{CRO} = 20$ kHz

θ_B (boost) = 65.5°

$G_A = 8.33$ (see equation 3)

$$G_A = \text{amplifier gain} = \frac{1}{\text{modulator gain } G_{PM} \text{ (at } f_{CRO})} \quad (3)$$

$$= \frac{1}{0.12} = 8.33$$

Overvoltage/Undervoltage Protection Using the TL7770-5 Supervisor Circuit

The TL7770-5 is used to sense overvoltage and undervoltage conditions at the 5-V output (see Figure 26). The undervoltage circuit begins operation when V_O attains a minimum voltage of 2.2 V during power-up and the RESET NO. 1 OUT and RESET NO. 2 OUT become active high to signal undefined operation. These reset outputs remain high until V_O exceeds their respective programmed threshold values for time delays (t_d), which are determined by external capacitors.

$$t_d = 40 \times 10^3 \times C \text{ where C is in farads and } t_d \text{ is in seconds}$$

choose

$$C20 = C21 = 0.001 \times 10^{-6} \text{ farads and}$$
$$t_{d1} + t_{d2} = 40 \times 10^{-6} \text{ seconds}$$

The RESET NO. 1 OUT (TRIP 1) signal to the microcomputer interrupt circuit (brown-out flag) is controlled by a threshold value of 4.55 V on the TL7770-5's internal R1/R2 divider.

$$V_{(TRIP\ 1)} = V_{REF} \times \frac{(R1 + R2)}{R2} = 1.5\ V \times \frac{(R1 + R2)}{R2} = 4.55\ V$$

The RESET NO. 2 OUT (TRIP 2) signal to the microcomputer interrupt circuit (black-out flag) is controlled by a threshold value of 4.2 V on the external R40/R41 divider.

$$V_{(TRIP\ 2)} = V_{REF} \times \frac{(R41 + R42)}{R41} = 1.5\ V \times \frac{(180\ k\Omega + 100\ k\Omega)}{100\ k\Omega} = 4.2\ V$$

RESET NO. 1 OUT and RESET NO. 2 OUT signals are both active low when V_O attains a minimum voltage of 1 V and both remain low until $V_{(TRIP\ 1)}$ and $V_{(TRIP\ 2)}$ threshold values are exceeded for the respective $t_{d(1)}$ and $t_{d(2)}$ delay times.

The overvoltage trip is programmed at 6.5 V by the R42/R43 divider and will trigger the TLC116F crowbar SCR2.

$$V_{OV\ (TRIP)} = V_{REF} \times \frac{(R42 + R43)}{R43} = 2.6\ V \times \frac{(150\ k\Omega + 100\ k\Omega)}{100\ k\Omega} = 6.5\ V$$

Any overvoltage condition that causes crowbar SCR2 to turn on also causes a signal to be concurrently sent to SCR1 that turns it on. The turned-on SCR1 provides base current to Q5. Q5 turns on and provides approximately 4 V to the TL598 dead-time control input which shuts down the power supply. This eliminates the need to heat sink the crowbar SCR and also prevents its possible destruction as a consequence of conducting continuous short-circuit current. To reset, the power supply must be turned off for a few seconds.

Operation of the overvoltage/undervoltage network is illustrated by the timing diagram shown in Figure 27.

DC-to-DC Converter Design Schematic

Figure 28 represents the completed design of a 100-kHz, 50-W, DC-DC converter that uses the TL598 control circuit.

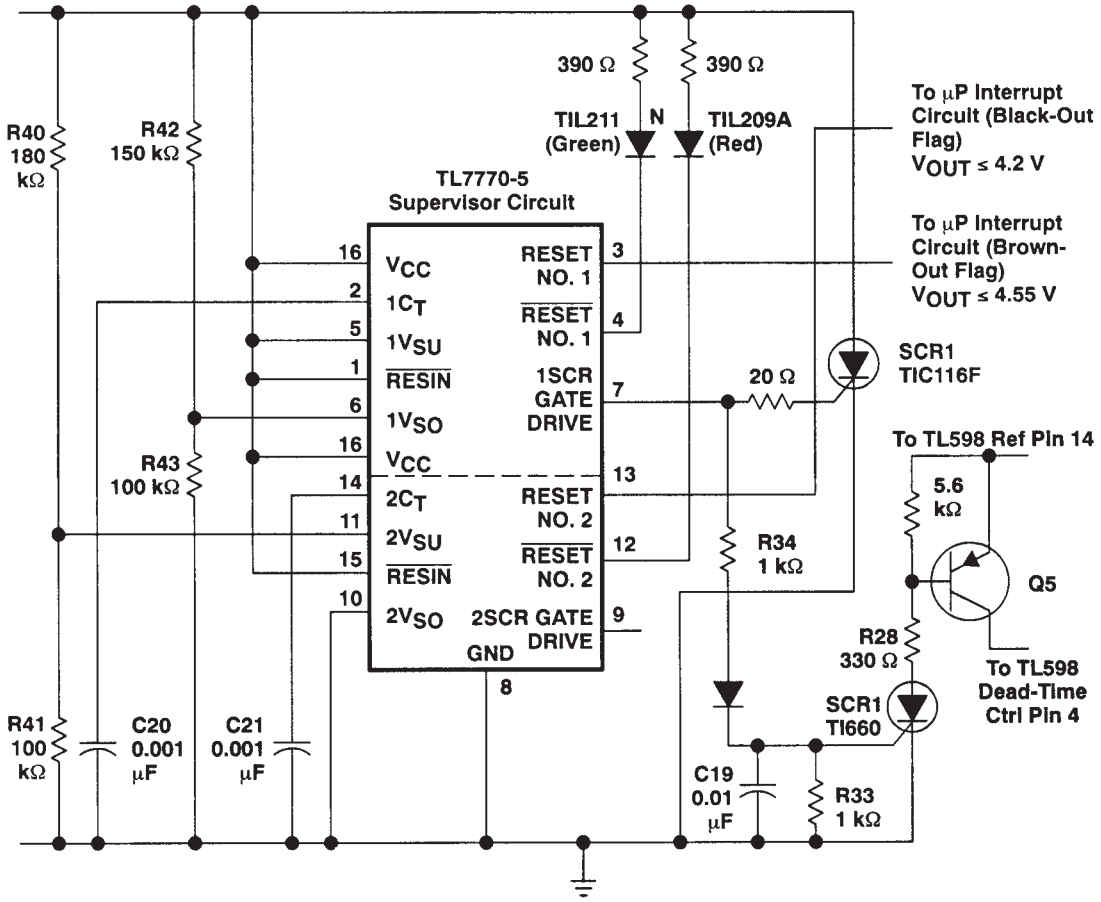


Figure 26. Overvoltage/Undervoltage Protection Circuits Using the TL7770-5

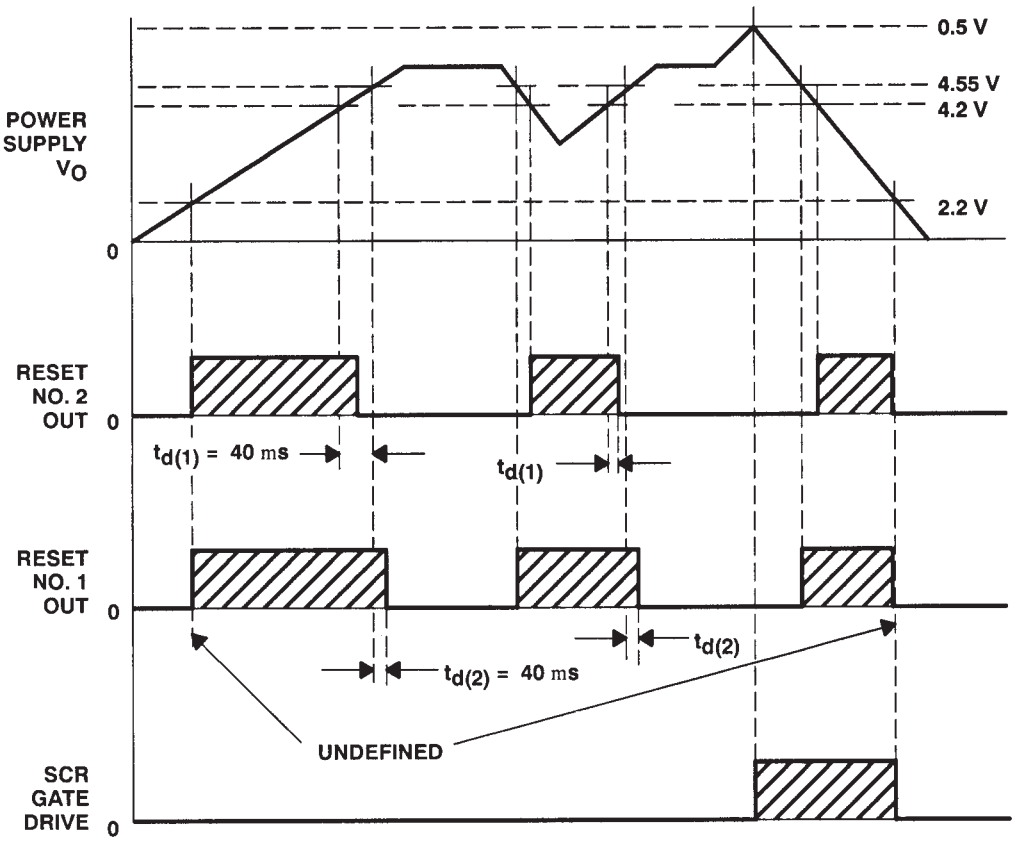
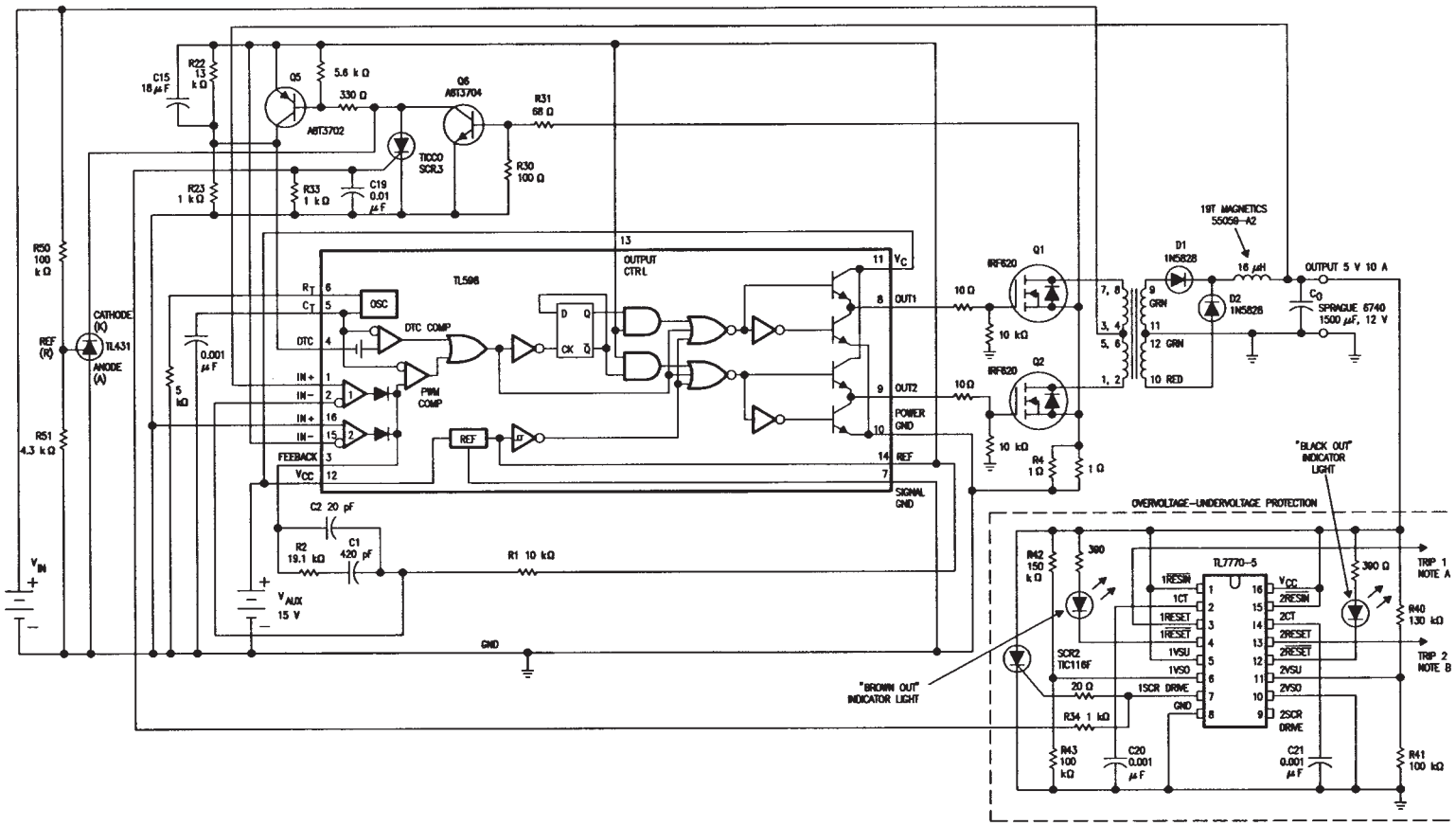


Figure 27. Overvoltage/Undervoltage Circuits Timing Diagram



NOTES: A. "Trip 1 Output" will be active high when power supply output ≥ 2.2 V ≤ 4.55 V. Trip 1 is connected to µP interrupt circuit, "Brown Out Flag".
B. "Trip 2 Output" will be active high when power supply output ≥ 2.2 V ≤ 4.2 V. Trip 2 is connected to µP interrupt circuit, "Black Out Flag".
C. SCR2 will turn on and "Crowbar" the filter capacitor C_O if power supply output exceeds 6.5 V.

Figure 28. 100-kHz, 50-W, DC-DC Design Using the TL598 Control Circuit

Measurements Results and Conclusions

Measurements of output and input regulation are made at the minimum input voltage of 42 V, the nominal input voltage of 48 V, and the maximum input voltage of 56 V. This is done while the load is changed from 0 to 10 A at each of the input voltage conditions. In addition, total input power is recorded at each of the specified conditions and the overall output power and power-supply efficiency is calculated and placed in Table 1 below:

Table 1. Measurement Results

V_I (V)	I_{LOAD} (A)	P_I (W)	P_O (W)	V_O (V)	EFF (%)
42	0	0.42	0	5.011	—
	1	7.75	5.01	5.010	64.7
	2	13.48	10.02	5.011	74.3
	3	19.13	15.03	5.011	78.6
	4	24.91	20.04	5.011	80.5
	5	31.10	25.06	5.012	80.6
	6	36.92	30.07	5.012	81.5
	7	43.49	35.08	5.012	80.7
	8	50.02	40.10	5.012	80.2
	9	56.21	45.10	5.011	80.2
	10	62.38	49.03	5.011	78.6
48	0	0.74	0	5.009	—
	1	7.63	5.01	5.009	65.7
	2	13.31	10.02	5.010	75.3
	3	19.04	15.03	5.010	78.9
	4	25.92	20.04	5.010	80.4
	5	30.79	25.05	5.010	81.4
	6	36.71	30.06	5.010	81.9
	7	43.06	35.08	5.011	81.5
	8	49.56	40.09	5.011	80.9
	9	55.72	40.10	5.011	80.9
	10	62.99	50.10	5.010	79.5
56	0	0.42	0	5.011	—
	1	7.10	5.01	5.010	66.8
	2	13.29	10.02	5.011	75.4
	3	18.54	15.03	5.011	79.7
	4	24.69	20.04	5.011	81.2
	5	30.42	25.06	5.011	82.4
	6	36.42	30.07	5.012	82.6
	7	42.71	35.08	5.011	82.1
	8	49.00	40.10	5.012	81.8
	9	55.28	45.11	5.012	81.6
	10	61.73	50.12	5.012	81.2

The input regulation equals 0.04% at I_{LOAD} = 10 A and V_I = 42 V to 56 V. The output regulation equals 0.04% at V_I = 42 V, 48 V, and 56 V with I_{LOAD} = 0 to 10 A. The 200-kHz ripple voltage at the 5-V output is measured as approximately 30 mV peak-to-peak, which meets the 125-mV design objective.

The overcurrent protection network described on page 22 works as specified and provides both short-circuit protection for the 10-A output and protection against transformer-core saturation.

The overvoltage and undervoltage protection networks for the input and output, described on pages 15 and 22, also works as specified and provides protection to meet all of the designed trip-voltage values.

In conclusion, the measurement results prove that the converter design example described in this report meets or exceeds all of the requirements of the converter specification.

Acknowledgment

The author, Joe Mings, wishes to thank Mr. Ira N. Frost of the Texas Instruments Linear Systems/ Automotive Lab for building the DC-DC converter described in this report and also for his most valuable technical suggestions and assistance on this project.

Also, thanks are given to Mr. Dennis Hahn, Mr. Fred Trafton, Mr. Darrell Whitten and Mr. Rick DeMars for their important technical contributions.

References

1. Venable, H. Dean, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis", *Proceedings of POWERCON 10*, pp H1-12.
2. Spencer, John, "Designing Switching Voltage Regulators with TL494", Texas Instruments Application Report, Bulletin CA-198.
3. Mings, Joe; Schwartz, Jim, "500-W/80-A, Off-the-Line, Half-Bridge Converter, Switching Power Supply", Texas Instruments Application Report, Bulletin SCA-209.

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